# 1st SEMESTER MODEL QUESTION PAPERS

**MTVL – 1.1**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**VLSI DESIGN TECHNIQUES**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions
All questions carry equal marks

I. a) Write on advantages of MOS transistor over Bipolar transistors.
b) Explain the basic structure, operation and drain current characteristics of a depletion type MOSFET.

2. a) Explain analytically the behavior of a CMOS inverter with its transfer characteristics.
b) Consider PFET that has a gate oxide thickness oft◦, = 60°A. The hole mobility is measured to be 220 $cm^2$/V-sec. and the aspect ratio is WI = 12/1. Assume that $V_{DD}$ = 3.3 V and VTp = 0.7 V. Calculate the process transconductance $K_p$ in units of mA/V2.

3. a) Explain about MOS SPICE model.
b) Describe about circuit characterization.

4. a) Discuss about circuit layout and simulation.
b) Distinguish between pass transistor logic and transmission gate logic.

5. a) Distinguish between static MOS design and dynamic MOS design.
b) Explain the steps for drawing NOR gate layout.

6. Sketch the logic gate symbolic representation of an JK Flip- flop using NAND gates. Give the truth table and describe the operation. Also sketch a CMOS circuit implementation

7. a) Write on input and output interface circuits.
b) Explain the blow:
i) Cross Talks
ii) Clock distribution
iii) Interconnect delays

8. a) Write on applications of BiCMOS Technology.
b) Explain the operation Basic BiCMOS Circuit

**MTVL – 1.2**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

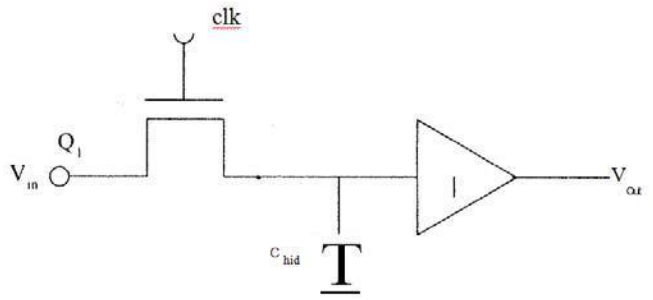
**ANALOG IC DESIGN**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions

All questions carry equal marks

1. a) Derive the relationship between $I_{ds}$ and $V_{ds}$ for an NMOS device.
   b) Compare CMOS and bipolar technologies.
2. a) What is current boosting? Explain the common source amplifier.
   b) Give the reasons why an open loop op-amp is not suitable for linear applications with necessary analysis.
3. a) Explain the current mirror operational amplifier.
   b) What are BiCMOS comparators? Derive the expression for Latch time in latched comparators.
4. a) Explain fully differential folded cascade OPAMP.
   b) Design a practical integration circuit using OP-AMP and explain its frequency response
5. a) Explain CMOS sample and hold ckt in detail.
   b) Explain Differential Operational Amplifier
6. a) Consider the sample and hold ckt shown in figure where $V_{th}$ is a 20 MHz band limited signal with a 2-$V_m$ amplitude. Assume that $P_{uk}$ is 100 MHz square wave having a peak amplitude of + 2.5 V with linear rise and fall times of 1.5 ns. What is maximum uncertainity of the sampling time.




   b) Write short notes on
      (i) Acquisition time
      ii) Aperture time
7. (a) What are the performance limitations for A/D and D/A converters? Explain.
   (b) Explain the first order active RC filters and first order switched capacitor filters.
8. Write short notes on
      i) Digital Decimation Fillets
      ii)Over sampling with and without noise shaping

**Elective I**
**MTVL – 1.3**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**Elective I : DIGITAL SIGNAL PROCESSING**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions

All questions carry equal marks

1. a) In an application signal received from one source from different paths has to be processed. Assuming the source is moving away from the receiver, suggest a suitable filter for this processing. (10)
   b) Name one optimization technique for a GIR filter. (4)

2. a) Show schematically how up sampling can be realized? (8)
   b) A signal f(4) is sampled at frequency $f_s$, what is the frequency domain characteristic of this has to be sampled at f, where f, is not a multiple off$_s$? (6)

3. a) With a block diagram, describe the operation of a digital filter bark used in speech processing. (8)
   b) Define the important parameters of a digital filter bark. (6)

4. a) Obtain the linear prediction equation for a sample S based on previous samples $S_i$. (8)
   b) Where are Toeplez matrices encountered in LPC? (6)

5. a) State the Schur algorithm and show its uses. (7)
   b) Compare DIT & DFT implementation. (7)

6. a) Obtain the relationship between autocorrelation arid the model parameters (7)
   b) Describe a floating point standard used in DSP (7)

7. a) Show the architecture of a typical DSP processor (7)
   b) How is the MAC used in DSP process? (7)

8. a) Explain the digital speech production model. (7)
   b) Describe a typical vocoder (7)

**MTVL – 1.3**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

# ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions
All questions carry equal marks

1. (a) List out the various Pipeline Hazards used in Microprocessor.
   (b) Compare Instruction level parallelism Architectures.

2. (a) List different types of 8086 hardware interrupts
   ( b) Explain any eight assembler directives of 8086 microprocessor.

3. (a) Give three examples for the following 8086 microprocessor instructions :String Instructions, Process Control Instructions, Program Execution Transfer Instructions and Bit Manipulation Instructions
   (b) How does one define and Call Macro parameters of 8086 microprocessor?

4. (a) Differentiate between 8086 and 8088.
   (b) Write an 8086 assembly language program to multiply two 16 bit unsigned numbers to provide a 32 bit results. Assume that the two numbers are stored in CX and DX.

5. (a) List out the problems associated with interfacing of a A/D Converters to the PC and Data acquisition.
   (b) Write a program using instruction set of 8086 to generate a continuous square wave with the period of 500 μs. Assume the system clock period in 325ns and use bit D0 to output the square wave.

6. (a) Explain the state transition diagram for Pentium processor bus cycle.
   (b) Describe the architecture and working of MC 68000 microprocessor.

7. (a) Explain the Architecture of 8051.
   (b) Mention the Application of MCS-51 and PIC microcontrollers.

8. Write short notes on the following
   a. Comparison of 8051 and 8052
   b. Pin description of Atmel microcontrollers

**Elective II**
**Model Question Paper**

**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering MTVL-1.4 : CPLD**

**AND FPGA Architecture and applications**

**Time: 3hrs Maximum** **Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1 . a) Distinguish between ROM's, PLAs and PALS.
b) Mention the features of Altera Flex logic-1000 series CPLD.

2. a) When is CPLD better suited than SPLD.
b) Give the Design Flow for xilinx FPGA's.

3. a) Give the routing architectures and logic Blocks of FPGA.
b) Give the architecture and salient features of optimized Reconfigurable cell Array (ORCA) of AT&T.

4. a) Why is it that PLDs are better than LCAs where the number of variables is large?
b) Describe the Xilinx 4000 series FPGAs.

5. a) Explain about Linked state Machines and one-Hot state machine.
b) Explain about the term Synchronization. Give its significance.

6. a) The reduced state table of a sequential machine has 12 rows. What is the minimum number of flip-flops needed to implement the machine?
b) With an example explain about one Hot design Method using ASMs.

7. a) Explain about Linked State Machines.
b) Explain the FSM architecture centered around shift registers.

8. Write notes on any TWO of the following.
a) Mentor Graphics EDA tool
b) ACTEL's and their speed performance.
c) Parallel adder design using FPGA.

**MTVL-1.4**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**Elective – II : VHDL MODELLING OF DIGITAL SYSTEMS**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions
All questions carry equal marks

1. (a) With neat sketch explain the digital system design approach using VHDL.
(b) What are the design verification tools available? Explain any one of them.

2. (a) Differentiate concurrent and sequential assignments used in VHDL. Give suitable example.
(b) Consider an example of one-bit full adder, explain the structural specification of hardware and give its structural description using VHDL.

3. Explain the following relevant to design organization with suitable example.
(a) Design Parameterization
(b) Design Consideration
(c) Design Libraries

4. What are the various sequential statements in VHDL? Explain the behavioral description of Wait Statement with relevant example.
(b) Define the term' State Machine'. With the aid of suitable logic diagram describe the importance of state machine in digital system design.

5. Draw the block diagram of CPU top-level design and describe its functionality using VHDL.

6. Describe the following design procedures used for system design using CAD Tools.
(a) Design Entry
(b) Simulation
(c) Synthesis

7. (a) What are the Subprograms in VHDL? Explain them in brief with suitable example.
(b) Differentiate predefined attributes and user defined attributes with respect to various features.

8. Write notes on any TWO of the following.
(a) Modeling a Test Bench
(b) MSI-Based Design

(c) Parwan CPU

**MTVL-1.4**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**Elective – II : ELECTRONIC DESIGN AUTOMATION TOOLS**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions
All questions carry equal marks

1. Explain in detail the different features of verilog language.

2. a) Explain the following synthesis for VHDL i) FSM synthesis (ii)) Memory synthesis

   b) Explain in detail the following simulation (i) Switch-level (ii) Transistor-level

3. Name different CAD tools for simulation and synthesis and explain them in detail.

4.a) Draw the PSPICE model for sample and hold circuit and explain.

   b) Design a two stage RC coupled amplifier and analyze it using PSPICE. Assume the data needed.

5. a) Give in detail the analysis of Up and Down converters.

   b) Explain in detail mixed signal simulator configurations.

6. Give in detail an overview of high speed PCB design.

7. a) Explain in detail orcad PCB design tools.

   b) Write short notes on Leonardo spectrum.

8. Write short notes on:

   a) Timing controls and delay in Verilog

   b) Formal verification procedure

# 2nd SEMESTER MODEL QUESTION PAPERS

**MTVL-2.1**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**DIGITAL SYSTEM DESIGN**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions

All questions carry equal marks

1. a) Describe about Hardware description language.
   b) What is a logic probe? What for it used and list different internal digital IC faults?

2. a) How does the ASM chart differ from a software flow chart? b) Distinguish between CPLD and FPGA.

3. a) Discuss **in** detail about reduction of state tables and state assignments.
   b) Explain about (i) Stuck at faults, (ii) Bridge faults, (iii) Temporary faults.

4. a) Explain the delay modeling for Gates with neat diagrams.
   b) Explain about D-algorithm in combinational circuits.

5. a) With example, explain the principle of Boolean difference method.
   b) Distinguish between PLA and PAL.

6. a) Design and realize a PLA circuit with four inputs $X_i$, $X_2$, X3 and $X_4$ and seven outputs 1)$_1$, $P_2$, $M_I$, 111$_2$, $m_3$, $m_4$ and $m_5$ that receives BCD code words and generates the corresponding code words.
   b) Distinguish between Mealy and Moore Machines.

7. a) Implement the Hazard free circuit for the following function:
   $f(A,B,C,D) = \cdot ABC + ABC + Ci5 + AC$
   b) Discuss about BIST scheme for PLD and CPI,D's

8. Write short notes on any TWO of the following:
   (i) Design for Testability
   (ii) PLA folding Algorithm COMPACT
   (iii ) Kohari algorithm

**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering**

**MTVL-2.2 : Algorithms for VLSI Design Automation**

**Time: 3hrs** **Maximum Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1. a) Explain about the VLSI Design Problem.
   b) Explain briefly Depth-first Search and Prim's Algorithm for Minimum Spanning Trees Related to Algorithms for VLSI design Automation.

2. a) Explain briefly the general purpose methods Dynamic Programming and Integer Linear Programming for combinational optimization.
   b) Write short notes on Genetic Algorithms.

3. a) Explain about the Kernighan-Lin Partitioning Algorithm
   b) Explain the routing problems in floor planning methods of VLSI design.

4. What is meant by modeling and simulation? Differentiate grate level and switch level modeling and simulation procedures with suitable example.

5. a) Discuss the basic issues and terminology employed in logic synthesis in VLSI design.
   b) Explain about ROBDD Principles with suitable example.

6. a)Explain about ASAP Scheduling and Force-directed Scheduling relevant to High-level logic synthesis.
   b) Write short notes on High-level transformations related High-level logic synthesis.

7. a) With suitable diagram explain new trends physical design cycle for FPGAs.
   b) Explain about Routing Algorithms for the Segmented Model.

8. a) Explain the MCM Routing Algorithms in detail.
   b) Write short notes on MCM physical design cycle.

**Elective -III**
**Model Question Paper**
**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering**

**MTVL-2.3 : Low Power VLSI Design**

**Time: 3hrs** **Maximum Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1. a) What are the limitations of Low power designing?
   b) Draw the cross-section diagram of BiCMOS structure of an npn bipolar transistor is added to a basic n-well CMOS process and explain it.

2. a) Draw the cross section of a transistor fabricated using the CDI process and explain how Isolation is obtained.
   b) Prove that in BiCMOS process the operating voltage is limited by the BVCEO.

3. a) What is the need for copper in SOI BiCMOS?
   b) Draw the cross-sectional view of SOI lateral BJT and write its electrical characteristics.

4. a) What are the features of MOSFET in Noise model?
   b) What are the limitations of MOS Device models?
   c) How Device current can be extracted ?

5. a) Draw the Two input NAND gate using BiCMOS logic gates and explain its operation with truth table.
   b) Draw the circuit diagram of BiCMOS buffer and explain its working.

6. a) Compare the conventional and advanced BiCMOS circuits.
   b) What is ESD? Design a ESD-free BiCMOS Inverter.

7. a) How to avoid feed through problems and race conditions in flip-flops?
   b) How pipe lining is used in C2MOS flip-flops?

8. a) Draw the circuit diagram of a CVSL style clocked SR latch with S and R as active high inputs and explain it.
   b) Explain how the quality of Latches and flip-flops is measured

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering**

**ELECTIVE-IV**

**MTVL-2.4 – Microcontrollers and Embedded Systems**

**Time: 3hrs** **Maximum Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1. (a) List and define the three main characteristics of embedded systems that distinguish such systems from other computing system. (2)

   (b) List and define the three IC technologies. What are the benefits of using each of the three different IC technologies. (4)

   (c) What is a Single-Purpose Processor? Design a custom Single-Purpose Processor? Explain with an example. (8)

2. (a) Explain the software development process of an embedded system. (7)

   (b) Enumerate the similarities and differences between a Microcontroller and Digital Signal Processor. (7)

3. (a) Given a 100MHz Crystal-Controlled Oscillator and a 32-bit and any number of 16-bit terminal counters. Design a relative clock that outputs the date and time down to milliseconds. You can ignore leap years. Draw a diagram and indicate terminal-count values for all counters. (9)

   (b) A watchdog timer uses two cascaded 16-bit up-counters is connected to an 11.981MHz oscillator. A time out should occur if the function watchdog-reset is not called within 5 minutes. What value should be loaded into the up-counter pair when the function is called. (5)

4. (a) Explain the cache impact on system performance with an example. (7)

   (b) Given the following three cache designs, find the one with best performance by calculating the average cost of access. Show all calculations.

   i. 4 Kbyte, 8-way set-associative cache with a 6% miss rate cache hit costs one cycle, cache miss cost 12 cycles.

   ii. 8 Kbyte, 4-way set-associative cache with a 4% miss rate cache hit costs two cycle, cache miss cost 12 cycles.

   iii. 16 Kbyte, 2-way set-associative cache with a 2% miss rate cache hit costs three cycle, cache miss cost 12 cycles. (7)

5. (a) Draw the timing diagram for a bus protocol that is handshaked non-addressed and transfers 8-bits of data over a 4-bit data bus. (7)

   (b) Explain the benefits an interrupt address table over fixed and vector interrupt methods. (7)

6. List the modifications made in Implementation: 2 (Microcontroller and CCDPP) and Implementation: 3 Microcontroller and CCDPP/ Fixed –Point DCT and discuss why each was beneficial in terms of performance. (14)

7. (a) Define the following terms: (7)

(i) Finite-state machines concurrent processor,

(ii) Real-time systems, and

(iii) Real-time operating systems.

(b) List three requirements of real-time systems and briefly describe each. Give examples of actual Real-time systems to support your arguments. (7)

8. Write notes on the following.

(a) Common Memory Types. (7)

(b) Stepper Motor Controllers. (7)

# 3rd SEMESTER MODEL QUESTION PAPERS

## Elective-V
## Model Question Paper

**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering**

**MTVL-3.1: System Modelling and Simulation**

**Time: 3hrs** **Maximum Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1. (a) Define system modelling and simulation.

   (b) Explain about discrete and distributed delays.

2. (a) Explain in detail system encapsulation.

   (b) Compare different simulation packages with programming languages.

3. (a) Discuss about standard Petrinet nomenclatures.

   (b) Explain alternative approach to modelling and simulation.

4. (a) Discuss about M/M/C queues.

   (b) Define Poisson process? List out the Poisson postulates and its properties.

5. (a) Discuss about random walks and draw the state-diagram for a four-node random walk with reflecting borders.

   (b) Explain system encapsulation.

6. (a) Explain in detail about alpha/Beta trackers.

   (b) Discuss about multi-dimensional optimization.

7. (a) Explain in detail about continuous time Markov process.

   (b) Explain about state machines.

8. (a) Discuss the techniques for increasing model validity and credibility.

   (b) Explain about queuing theory and types of queues.

**MTVL-3.1**

**Model Question Paper**

**M.Tech (VLSI) Degree Examination – First Semester**

**Electronics and Communication Engineering**

**Elective – II : EMI / EMC**

**Time: 3hrs** **Maximum Marks : 70**

Answer any FIVE questions
All questions carry equal marks

1. (a) What is the effect of a lighting strike in the vicinity of a VHP receiver and how can it be minimized? (10)
   (b) What are the sources of atmospheric EMO? (4)

2. (a) What are the standards of RF interference? (7)
   (b) Explain how sun spot activity may affect communication? (7)

3. (a) A telephone cable contains 1200 wires of gauge 42 and are enclosed in a core. What are the possible interferences and how can they be minimized? (6)
   (b) A power amplifier of a transmitter radiates 100 KW at 1200 MHz. If it is operating under class C what is its affect on electronic equipment in the vicinity? (8)

4. (a) What are the difference between E & H field interferences? (7)
   (b) What is meant by EM compatibility? (7)

5. (a) Describe the various principles and types of shielding techniques. Give the Design methodologies of shielding and what do you mean by shielding effectiveness? (8)
   (b) What is a Faraday cage? (6)

6. (a) What is Electra static Discharge and what is its effect in microelectronic circuits ? (7)
   (b) What precautions are to be observed when embedding IC's into pacemakers etc? (7)

7. (a) What are the various types of Groundings to be adopted when installing a medical diagnostic machine life an EEG? (8)
   (b) What are the radiation points permitted for equipment like a X-ray machine? (6)

8. (a) What is Common mode coupling encountered in connections? (7)
   (b) What materials are used for sealing RF equipment and how do they operate ? (7)

**Open Elective**
**Model Question Paper**

**M.Tech (VLSI) Degree Examination – Second Semester**

**Electronics and Communication Engineering**

**MTVL-3.2 – CELLULAR AND MOBILE COMMUNICATIONS**

**Time: 3hrs** **Maximum Marks : 70**

**Answer any Five Questions. All Questions carry equal marks**

1. Discuss sequence of steps in initiating a cell from one cell user to the others.

2. (a)What is meant by frequency reuse concept and what are the important points to be considered in frequency reuse concept.
   (b) Discuss near field and far field problems in cellular systems.

3. Explain clearly forward and reverse channels for CDMA systems.

4. (a) Discuss clearly the important parameters of multipath channels. (b)Discuss important indoor propagation models.

5. Discuss important power control strategies used in mobile communications.

6.Discuss different methods to improve the capacity and coverage of existing cellular system.

7. (a) Discuss the advantages of space diversity antennas used at cell site.
   (b) Discuss different hand-off strategies.

8. Write short notes on the following.
   (a) Rake receiver
   (b) Personal mobile satellite communications
   (c) LEO