M.Tech (VLSI), B.Tech+M.Tech(5/6 and 6/6), Two Year (Four Semesters)

Scheme to be valid with effect from the admitted batch of 2019 – 2020

I-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL1.1	VLSI Design Techniques	3	-	70	30	100	3
MTVL1.2	Analog IC design	3	-	70	30	100	3
MTVL1.3	Elective – I (Digital Signal Processing/ Application Specific Integrated Circuit(ASIC)/ Hardware Software Co Design/ Advanced Microprocessors & Microcontrollers)	3	-	70	30	100	3
MTVL1.4	Elective – II (CPLD and FPGA Architecture & Applications / VHDL Modelling of Digital Systems/EDA Tools)	3	-	70	30	100	3
MTVL1.5	Research Methodology & IPR	3	-	70	30	100	2
MTVL1.6	Audit Course	3	-	70	30	100	0
MTVL1.7	HDL Programming LAB-I	-	3	50	50	100	2
MTVL1.8	Analog IC Design LAB	-	3	50	50	100	2
		18	6	520	280	800	18

II-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL2.1	Digital System Design	3	-	70	30	100	3
MTVL2.2	Algorithms for VLSI design automation	3	-	70	30	100	3
MTVL2.3	Elective – III (Low Power VLSI Design/ Wireless Communication and networks/ RF& Microwave Integrate Circuits)	3	-	70	30	100	3
MTVL2.4	Elective – IV (Microcontroller and Embedded Systems/ Digital Systems Testing & Testable Design/ DSP Processors and Architectures)	3	-	70	30	100	3
MTVL2.5	Audit Course	3	-	70	30	100	2
MTVL2.6	HDL Programming LAB-II	-	3	50	50	100	2
MTVL2.7	Mixed Signal Simulation LAB	-	3	50	50	100	2
MTVL2.8	Mini Project with Seminar	-	3	-	100	100	2
		15	9	450	350	800	18

III-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL3.1	Elective – V System Modeling and Simulation/ / Cellular & Mobile Communications/ EMI/EMC	3	-	70	30	100	3
MTVL3.2	Open Elective Business Analytics Industrial Safety Operational Research Cost Management of Engineering Projects	3	-	70	30	100	3
MTVL3.3	Dissertation- I / Industrial Project	-	-	100	--	100	10
		6	-	240	60	300	16

IV-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL4.1	Dissertation-II	-	-	100	-	100	16
		-	-	100	-	100	16

Audit Course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

VLSI DESIGN TECHNIQUES

Credits : 3

Subject Code :MTVL – 1.1 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT- I

INTRODUCTION: Basic Principle of MOS Transistor, Introduction to Large Signal MOS Models(Long Channel) For Digital Design.

UNIT –II

THE MOS INVERTER, LAYOUT AND SIMULATION: Inverter principle, Depletion andenhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. MOS SPICE Model, Device Characterization, Circuit Characterization, Interconnects and Simulation. MOS Device Layout, Transistor Layout, Inverter Layout, CMOS Digital Circuits Layout & Simulation

UNIT- III

COMBINATIONAL MOS LOGIC DESIGN: Static MOS design; Complementary MOS,Rationed logic, Pass Transistor logic, complex logic circuits, Dynamic MOS Design, Dynamic Logic Families and Performances.

UNIT –IV

SEQUENTIAL MOS LOGIC DESIGN: Static Latches, Flip Flops and Registers, DynamicLatches and Registers, CMOS Schmitt trigger, Monostable Sequential Circuits, Astable Circuits, Memory Design, ROM and RAM Cells Design

UNIT –V

INTERCONNECT AND CLOCK DISTRIBUTION: Interconnect Delays, Cross Talks, ClockDistribution. Introduction to Low- power Design, Input and Output Interface circuits.

UNIT-VI

BICMOS LOGIC CIRCUITS: Introduction, BJT Structure and Operation, Basic BiCMOSCircuit behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications

TEXT BOOKS:

1. Kang &Leblebigi “CMOS Digital IC Circuit Analysis & Design”- McGraw Hill, 2003
2. Rabey, “Digital Integrated Circuits Design”, Pearson Education, Second Edition, 2003

REFERENCE:

1. Weste and Eshraghian, “Principles of CMOS VLSI design” Addison-Wesley, 2002

ANALOG IC DESIGN

Credits : 3

Subject Code: MTVL – 1.2 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT- I

INTEGRATED CIRCUIT DEVICES AND MODELLING: MOS Transistors, AdvancedMOS Modeling, Bipolar Junction Transistors, Device Model Summary, SPICE Modelling Parameters.

UNIT-II

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: Simple CMOS CurrentMirror, Common Source, Source-Follower, Common Gate Amplifier, High-Output-Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response.

UNIT –III

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOSOperational Amplifier, Feedback and Operational Amplifier Compensation, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

UNIT –IV

ADVANCED CURRENT MIRRORS AND OPERATIONAL AMPLIFIERS: AdvancedCurrent Mirror, Folded–Cascade Operational Amplifier, Current-Mirror Operational Amplifier, Fully Differential Operational Amplifiers, Common-Mode Feedback Circuits, Current-Feedback Operational Amplifiers.

UNIT-V

SAMPLE AND HOLD , SWITCHED-CAPACITOR CIRCUITS: MOS Sample-and-Hold Basics, CMOS Sample and Hold Circuits, Bipolar and BiCMOS Sample and Holds.Basic Operation and Analysis, First-Order and Biquad Filters, Charge Injection, Switched-Capacitor Gain Circuits, Correlated Double-Sampling Techniques, Other Switched-Capacitor circuits.

UNIT- VI

DATA CONVERTERS: Ideal D/A & A/D Converters, Quantization Noise, PerformanceLimitations, Nyquist-Rate D/A Converters: Decoder Based Converters, Binary-Scaled Converters, Hybrid Converters, Nyquist-Rate A/D Converters, Integrating, Successive-Approximation, Cyclic Flash Type, Two-Step A/D Converters, Interpolating A/D Converters, Folding A/D Converters and Pipelined A/D Converters. Over Sampling with and without Noise Shaping, Digital Decimation Filter, Higher-Order Modulators, Bandpass Oversampling Converter

TEXT BOOKS:

1. I.D.A.JOHN & KEN MARTIN; Analog Integrated circuit design. John Wiley,1997

REFERENCE:

1. GREGOLIAN & TEMES: Analog MOS Integrated Circuits, John Wiley, 1986

Elective-I

DIGITAL SIGNAL PROCESSING

Credits : 3

Subject Code :MTVL – 1.3 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT-I

ADVANCED DIGITAL FILTER DESIGN TECHNIQUES:Multiple Band Optimal FIRFilters, Design of Filters with Simultaneous Constraints in Time and Frequency Response, Optimization Methods for Designing IR Filters, Comparison of Optimum FIR Filters and Delay Equalized Elliptic Filters.

UNIT-II

MULTI-RATE DIGITAL SIGNAL PROCESSING:The basic sample rate alteration – Time – Domain Characterization, Frequency – Domain Characterization: Cascade Equivalences, Filters in Sampling Rate Alteration Systems.

UNIT-III

DIGITAL FILTER BANKS AND OPTIMUM LINEAR FILTERS: Analysis of DigitalFilter Banks and their Applications, Multi Level Filter Banks, Estimations of Spectra from Finite – Duration Observation of Signals , Forward and Backward Linear Prediction, AR Lattice and ARMA Lattice – Ladder Filters, Wieners Filters for Filtering on Prediction.

UNIT-IV

DIGITAL SIGNAL PROCESSING ALGORITHMS: The Goertzel Algorithm, The Chirpz -Transform Algorithm, The Levinson – Durbin Algorithms, The Schur Algorithm, and other Algorithms, Computations of the DFT, Concept of Tunable Digital Filters.

UNIT-V

SIGNAL PROCESSING HARDWARE AND FFT ARCHITECTURES AND PROCESSORS: Multipliers, Dividers, Different Forms of FIR Hardware, Multiplexing, DTTR, TDM to FDM Translator, Realization of Frequency Synthesizer. FFT Hardware Realization, Different FFT Architectures, Special FFT Processors, Convolvers, Lincoln Laboratory FDP and the Compatible Computer Configurations

UNIT-VI

APPLICATIONS OF DSP:Speech and DTMF Systems: Model of Speech Production, SpeechAnalysis –Synthesis System Vocoder Analyzers and Synthesizers, Linear Prediction of Speech and DTMF System.

TEXT BOOKS:

1. Theory and Applications of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold, PHI.
2. Digital Signal Processing. Principles, Algorithms, and Applications by John G. Proakis and Dimitris G. Manolakis, PHI, 1997.

REFERENCE:

1. Digital Signal Processing, A Computer – Based approach, by Sanjit K. Mitra, Tata Mc Graw-Hill, 1998

Elective-I

APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASIC)

Credits : 3

Subject Code :MTVL – 1.3 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT- I

Introduction to ASICs – Types of ASICs, Design flow, Economics of ASICs, ASIC Cell Libraries, CMOS Logic, CMOS Design Rules, Logic Cells, I/O Cells, Cell Compilers.

UNIT- II

ASIC Library Design – Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Cell Design, Programmable ASICs, Programmable ASIC Logic Cells, Programmable ASIC I/O Cells, Programmable ASIC Interconnect, Programmable ASIC Design Software.

UNIT -III

Low-level Design Entry, Schematic Entry, Low-Level Design Languages, PLA Tools, EDIF, An overview of VHDL and Verilog, Logic Synthesis, Simulation. ASIC Construction, Floor Planning and Placement.

UNIT- IV

CMOS System Core Studies: Dynamic Warp Processors: Introduction, The Problem, The Algorithm, A Functional Overview, Detailed Functional Specification, Structural Floor Plan, Physical Design, Fabrication, Hierarchical Layout And Design Of Single Chip 32 Bit CPU: Introduction, Design Methodology, Technology Updatability And Layout Verification

UNIT -V

Practical Realities and Ground Rules: Further Thoughts on Floor Plans/Layout, Floor Plan Layout of The Four Bit Processors, Input/output (I/O) Pads, “Real estate”, Further Thoughts on System Delays, Ground Rules for Successful Design, Scaling of MOS Circuits.

TEXTBOOK:

1. Application Specific Integrated Circuits by J.S. Smith, Addison Wesley, 1997.

REFERENCES:

1. Basic VLSI Design : Systems and Circuits, Doublas A. Pucknell& Kamran Eshraghian, Prentice Hall of India Private Ltd., New Delhi, 1989.
2. VLSI Design Techniques for analog and digital circuits, R.L. Geiger, P.E. Allen & N.R. Streder, McGraw Hill Int. 1990.

Elective-I

ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Credits : 3

Subject Code: MTVL – 1.3 **Max. Marks :**70
I – Semester **Sessionals :**30

Unit –I :

8086 / 8088 Microprocessor, Architecture and Addressing Modes. Instructions and assembly Language programming. Macro Assembler MASM and Advanced Programming.

Unit –II:

Interrupts of 8086 / 8088 and DOS Interrupt 21h functions. Interfacing A/D converters to the PC and data acquisition. Interfacing D/A converters and waveform generation.

Unit – III:

80286, 80386, 80486 and Pentium Microprocessors. Motorola 68000, 68020 and 68030 Microprocessors.

Unit –IV: General Microcontrollers

Introduction to the 8051 and 8052 Microcontrollers, features, architectures, memory organization, addressing modes, instruction set, assembly programming, software development tools, parallel I/O ports, interrupts, timers/counters, serial communication, data and control transfer operations, serial data transmissions, programming and interfacing using 8051.

Unit –V: Atmel Microcontrollers

Introduction to Atmel microcontrollers (89CXX and 89C20XX), Architecture overview of Atmel 89C51, pin description of Atmel microcontrollers, using flash memory devices, Atmel 89CXX and Atmel 89C20XX, Applications of MCS-51 and Atmel 89C51 and 89C2051 microcontrollers.

Unit –VI: PIC Microcontrollers

An introduction to PIC microcontrollers, PIC 8 series and PIC 16 series microcontrollers and PIC family of microcontrollers (16C8X/7X, 16F84A, 12F50X and 16F8XX), architecture, instruction set, programming using assembly language and C languages of the PIC microcontrollers, interfacing PIC Microcontrollers to the other devices, applications of PIC microcontrollers.

Text Books:

1. Microprocessor and Interfacing by Douglas V. Hall, McGraw Hill International Edition, 1992.
2. The Intel Microprocessor 8086 / 8088, 80186, 80286, 80386 and 80486 by Barry B. Brey, PHI, 1998.

References:

1. Assembly Language Programming the IBM PC by Alan R. Miller, Sybex INC, 1987.
2. 68000 Microprocessors by Walter A. Tribel and Avtar Singh, PHI, 1991.
3. Microcontrollers –Theory and Applications –by Ajay V Deshnukh –TMH

Publications.
4. The 8051 Microcontroller Architecture, Programming and Applications by Kenneth Ayala, Thomson Publishers

Elective-II

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Credits : 3

Subject Code :MTVL – 1.4 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT –I

Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA – Features, Architectures,Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT-II

CPLDs: Complex Programmable Logic Devices: Altera series – Max 5000/7000 series andAltera FLEX logic- 10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI's architectures – 3000 series – Speed performance and in system programmability.

UNIT – III

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow,technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-IV

Finite State Machines (FSM): Top Down Design, State Transition Table , State assignmentsfor FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine. Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study

UNIT- VI

Design Methods and System Level Design: One –hot design method, Use of ASMs in one-hot design method, Applications of one hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

UNIT – VIII

Case studies: Design considerations using CPLDs and FPGAs of parallel adder cell, paralleladder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.

3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad, 1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

Elective-II

VHDL MODELLING OF DIGITAL SYSTEMS

Credits : 3

Subject Code :MTVL – 1.4 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT I
INTRODUCTION

An Overview Of Design Procedures Used For System Design Using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples Using Commercial PC Based On VHDL Elements Of VHDL Top Down Design With VHDL Subprograms. Controller Description VHDL Operators.

UNIT II
BASIC CONCEPT IN VHDL

Characterizing Hardware Languages, Objects And Classes, Signal Assignments, Concurrent And Sequential Assignments. Structural Specification Of Hardware: Parts Library Wiring Of Primitives, Wiring Interactive
Networks, Modeling A Test Bench Binding Alternative Top Down Wiring.

UNIT III
DESIGN ORGANIZATIN AND PARAMETERIZATION

Definition And Usage If Subprograms, Packaging Parts And Utilities, Design Parametrization, Design Configuration, Design Libraries, Utilities For High –Level Descriptions-Type Declaration And Usage, VHDL Operators, Subprogram Parameter Types And Overloading, Other Types And Type Related Issues, Predefined Attributes, User Defined Attributes, Packing Basic Utilities.

UNIT IV
DATA FLOW DESCRIPTION IN VHDL

Multiplexing And Data Selection, State Machine Description, Open Collector Gates, Three State Bussing AGeneral Data Flow Circuit, Updating Basic Utilities. Behavioral Description Of Hardware: Process Statement Assection Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.

UNIT V
CPU MODELLING FOR DESCRIPTION IN VHDL

Parwan CPU, Behavioural Description OfParawan, Bussing Structure, Data Flow Description Test Bench For The Parwan CPU. A More Realistic Parwan. Interface Design And Modeling. VHDL As A Modelling Language.

TEXT BOOKS:

1. Z.NAWABI : VHDL Analysis And Modelling Of Digital Systems. (2/E), Mcgraw Hill, (1998)

REFERENCE:

1. PERRY : VHDL, (3/E) Mcgraw Hill 10

Elective –II

ELECTRONIC DESIGN AUTOMATION TOOLS

Credits : 3

Subject Code :MTVL – 1.4 **Max. Marks :**70
I – Semester **Sessionals :**30

UNIT I
IMPORTANT CONCEPTS IN VERILOG:
Basics Of Verilog Language, Operators, Hierarchy, Procedures And Asignments, Timing Controls And Delay. Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, other Verilog Features.

UNIT II
SYNTHESIS AND SIMULATION USING HDLS:
Verilog And Logic Synthesis. VHDL And Logic Synthesis, Memory Synthesis,FSMSynthesis,Memory Synthesis, Performance-Driven Synthesis. Simulation-Types Of Simulation, Logic Systems Working Of Logic Simulation,Cell Models, Delay Models State Timing Analysis,Formal Verification, Switch-Level Simulation Transistor-Level Simulation. CAD Tools For Synthesis And Simulation Modelism And Leonardo Spectrum(Exemplar).

UNIT III
TOOLS FOR CIRCUIT DESIGN AND SIMULATION USING PSPICE:
Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits Etc, And Digital System Building Blocks, Design And Analysis Of Analog And Digital Circuits Using PSPICE.

UNIT IV
AN OVER VIEW OF MIXED SIGNAL VLSI DESIGN:
Fundamentals Of Analog And Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAE Environments, Analyses Of Analog Circuits Eg.A/D, D/A Converters, Up And Down Converters, Companders Etc.

UNIT V
TOOLS FOR PCB DESIGN AND LAYOUT:
An Overview Of High Speed PCB Design, Design Entry, Simulation And Layout Tools For PCB. Introduction ToOrcad PCB Design Tools.

TEXTBOOKS

1. J.Bhaskar, A Verilog Primer, BSP, 2003.
2. J.Bhaskar, A Verilog HDL Synthesis BSP, 2003
3. M.H.RASHID:SPICE FOR Circuits And Electronics Using PSPICE (2/E)(1992) Prentice Hall.

REFERENCES

1. ORCAD: Technical Reference Manual ,Orcad, USA.
2. SABER: Technical Reference Manual, Analogy Nic, USA.
3. M.J.S.SMITH :Aplication-Specific Integrated Circuits(1997). Addison Wesley
4. J.Bhaskar, A VHDL Synthesis Primer, BSP, 2003.

RESEARCHMETHODOLOGY AND IPR

Credits: 2

Subject Code: MTVL – 1.5 **Exam Marks:** 70

Semester-I **Sessional:** 30

AUDIT COURSE

Credits: 0

Subject Code: MTVL – 1.6 **Exam Marks:** 70

Semester-I **Sessional:** 30

HDL PROGRAMMING LABORATORY-I

Credits: 2

Subject Code: MTVL – 1.7 **Max. Marks:** 100
I – Semester

ANALOG IC DESIGN LABORATORY-I

Credits: 2

Subject Code: MTVL – 1.8 **Max. Marks:** 100
I – Semester

DIGITAL SYSTEM DESIGN

Credits : 3

Subject Code :MTVL –2.1 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT – I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language andcontrol sequence method, Reduction of state tables, state assignments.

UNIT – II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequentialcircuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT – III

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transitionand intermittent faults. TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT – IV

TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transitioncount testing, Signature analysis and testing for bridging faults.

UNIT – V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and faultdetection experiment. Machine identification, Design of fault detection experiment.

UNIT – VI

PROGRAMMING LOGIC ARRAYS AND ASYNCHRONOUS SEQUENTIAL MACHINE: Design using PLA's, PLA minimization and PLA folding. Fault models, Testgeneration and Testable PLA design. Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards

TEXT BOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. NolmanBalabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition
2004.

REFRENCES:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition. 4

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Credits : 3

Subject Code :MTVL – 2.2 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT- I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools,Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems

UNIT- II

GENERAL PURPOSE MTHODS FOR COMBINATIONAL OPTIMIZATION:Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, LocalSearch, Simulated Annealing, Tabu search, Genetic Algorithms, Layout Compaction, Placement, Floorplanning and Routing Problems, Concepts and Algorithms.

UNIT- III

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch levelmodeling and simulation

UNIT- IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis, Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspectsofAssignment problem, High – level Transformations

UNIT –V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Designcycle for FPGA's partitioning and Routing for segmented and staggered models.

UNIT –VI

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physicaldesign cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, John wiley& Sons (Asia) Pvt.Ltd. 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer International Edition, 2005

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

Elective III
LOW POWER VLSI DESIGN

Credits: 3

Subject Code: MTVL – 2.3 **Max. Marks:** 70
II – Semester **Sessionals :**30

UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low powerdesign, limitations, Silicon-on-Insulator.

UNIT II
MOS/BiCMOS PROCESSES: Bi CMOS processes, Integration and Isolationconsiderations, Integrated Analog/Digital CMOS Process. Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT III
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT IV
CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates.Performance evaluation

UNIT V
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advancedBiCMOS Digital circuits. ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation

UNIT VI
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusufleblebici 3rd edition TMH2003 (chapter 11)
3. VLSI DSP systems, Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

Elective-III

WIRELESS COMMUNICATIONS AND NETWORKS

Credits : 3

Subject Code :MTVL – 2.3 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT -I

WIRELESS COMMUNICATION AND SYSTEM FUNDAMENTALS: Introduction toWireless Communication Systems, Examples of Wireless Communications, Comparisons of Common Wireless Communication Systems, Trends in Cellular Radio and Personal Communications, Cellular Concepts, Frequency Reuse, Handoff Strategies, Interference and System Capacity, Trucking and Grade Of Service, Improving Coverage & Capacity In Cellular Systems.

UNIT-II

MULTIPLE ACCESS TECHNIQUES FOR WIRELESS COMMUNICATION: FDMA,TDMA, SSMA (FHMA/CDMA/Hybrid Techniques) SDMA Technique (As Applicable to Wireless Communications), Packet Radio Access Protocols, CSMA Protocols, Reservation Protocols, Capture Effect in Packet Radio, Capacity of Cellular Systems.

UNIT-III

WIRELESS NETWORKING: Introduction, Differences Between Wireless and FixedTelephone Networks, Traffic Routing in Wireless Networks, Circuit Switching, Packet Switching, The X.25 protocol**.**

UNIT-IV

Wireless Data Services, Cellular Digital Packet Data (CDPD), Advanced Radio Data Information Systems (ARDIS), RAM Mobile Data (RMD), Common Channel Signaling (CCS), Broad Band ISDN and ATM, Signaling System .No.7 (SS7), Network Services Part (NSP), SS7 User Part, Signaling Traffic in SS7, SS7 Services, Performance of SS7.

UNIT-V

MOBILE IP AND WIRELESS APPLICATION PROTOCOL: Mobile IP Operation ofMobile IP, Co-located Address, Registration, Tunneling, WAP Architecture, Overview, WML Scripts, WAP Service, WAP Session protocol, Wireless Transaction, Wireless Datagram,Infrared LAN's, Spread Spectrum LAN's, Narrowband Microwave LAN's, IEEE 802 Protocol Architecture, IEEE 802 Architecture and Services, 802. 11 Medium Access Controls, 802.11 Physical Layers.

UNIT-VI

BLUE TOOTH AND MOBILE DATA NETWORKS: Overview, Radio Specification,Baseband Specification, Links Manager Specification, Logical Link Control and Adaptation Protocol, Introduction to WLL Technology, Introduction, and Data Oriented CDPD Network, GPRS and Higher Data Rates, Short Messaging Service in GSM, Mobile Application Protocol.

TEXT BOOKS:

1. Wireless communication and Networking -William Stallings, PHI, 2003
2. Wireless Communications, Principles, Practice - Theodore, S. Rappaport, PHI, 2nd Edition, 2002.

REFERENCES:

1. Wireless Digital Communications-Karnilofeher,PHI, 1999.
2. Principles of Wireless Networks - Kavehpahlaven and P.Krishna Murthy, Pearson Education, 2002

Elective-III

RF AND MICROWAVE INTEGRATED CIRCUITS

Credits : 3

Subject Code :MTVL – 2.3 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT-I

Analysis and Design of RF and Microwave Lines – Review of Transmission Lines, Parallel Plate Transmission Lines, Low -Frequency Solution, High Frequency Solution,

UNIT–II

Strip Line And Micro Strip Transmission Lines, Low Frequency Solution, High Frequency Properties Of Micro Slot Line, Co Planer Wave Guides, Spiral Inductors – Capacitors.

UNIT–III

Microstrip/Stripline Based Filters. Resonators, Plane Shifters, Micro Strip Based Gyrators, Circulators And Isolators, Directional Couplers.

UNIT–IV

Microwave Active Devices – Microwave Transistors, GaAs FETS (Structures, Equivalent Circuit), Low Noise Amplifiers, Power Amplifiers, Oscillators, Detect5ors, Mixers, Modulators and Switches.

UNIT-V

Technology of MICS: Deposition Techniques – Vacuum Evaporation – Vacuum Sputtering Ion Planting. MBE (molecular Beam Epitaxy) – Photo Lithography, Mask Preparation, Thick Film Technology, GaAs Technology.

UNIT–VI

MIC Packaging: Component Attachment, Bonding Techniques, Solder Reflow Techniques, Input/Output Terminations, Testing.

TEXT BOOKS:

1. Microwave Engineering – Prof. G.S.N Raju, I.K. International Publication.
2. I.Kneppo and J. Fabian, “Microwave Integrated Circuit”, London: Chapman & Hall, (1994).
3. M.W.Medley, “Microwave and RF circuit: Analysis, Synthesis and Design”, Artech House, (1993).

REFERENCES:

1. R.Goyal, “Monolithic Microwave Integrated Circuit: Technology & Design”, Artech House, (1989).
2. Y.Konishi, “Microwave Integrated Circuit”, Dekker, New York: Marcel Dekker, (1991).

Elective-IV

MICROCONTROLLERS AND EMBEDDED SYSTEMS

Credits: 3

Subject Code :MTVL – 2.4 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT-1

INTRODUCTION: Embedded Systems overview, Design Challenge, ProcessorTechnology, IC Technology, Design Technology, Trade-offs.

UNIT-II

CUSTOM SINGLE-PURPOSE PROCESSORS (HARDWARE): Introduction,Combinational logic, Sequential logic, Custom Single-Purpose Processor Design, RT-Level Custom Single-Purpose Processor Design, Optimizing Custom Single-Purpose Processors.

UNIT-III

GENERAL PURPOSE PROCESSORS (SOFTWARE): Introduction, Basic Architecture,Operation, Programmer's view, Development Environment, Application-Specific Instruction-set Processors, Selecting a Microprocessor.

UNIT-IV

MEMORY: Introduction, Memory types, Memory Hierarchy and Cache, Advanced MemoryInterfacing: Communication Basics, Memory Access, I/O addressing, Interrupts, DMA, Arbitration, Multilevel Architecture, Protocols.

UNIT-V

MICROCONTROLLERS: Review of 8051 Microcontroller Architecture &Programming**.**Peripherals: Timers, Counters and Watchdog Timers, UART, Pulse width Modulators, LCD Controllers, Stepper Motor Controllers, Analog to Digital Converters, Real-Time Clocks. Digital Camera Introduction, Specifications, Design.

UNIT-VI

STATE MACHINE AND CONCURRENT PROCESS MODELS: Introduction, ModelsVs Languages, Text Vs Graphics, Textual Languages Vs Graphical Languages, An Example, A Basic State Machine Model, FSM with Data Path Model, FSMD Using State Machines, Concurrent Process Model, Communication among Processes.

TEXT BOOKS:

1. Embedded System Design: A Unified Hardware/Software Introduction By Frank vahid / Tony Givargis John wiley& sons
2. The 8051 Microcontroller & Embedded Systems By Muhammad Ali Mazidi& Janice GillispieMazidi PHI

REFERENCES:

1. Embedded Systems Architecture, Programming and Design By RajKamal TMH
2. Embedded Software Priner By Simon.
3. The 8051 Microcontroller: Architecture, Programming & Applications. By Kenneth J.AyalaPenram International. 2nd edn.

Elective-IV

DIGITAL SYSTEMS TESTING AND TESTABLE DESIGN

Credits: 3

Subject Code: MTVL – 2.4 **Max. Marks:** 70
II – Semester **Sessionals:** 30

UNIT- I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) SIMULATIONS: Fundamentals, Modeling Digital Circuits at Logic Level, Register Leveland Structural Models. Levels of Modeling. Types of Simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT- II

FAULT MODELING: Logic fault models, Fault detection and redundancy, Faultequivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for combinational circuits.

UNIT- III

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation(ATPG/ATG) For SSFs In Combinational And Sequential Circuits ,Functional Testing With Specific Fault Models .Vector Simulation – ATPG Vectors ,Formats, Compaction And Compression ,Selecting ATPG Tool

UNIT- IV

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan ArchitecturesAnd Testing – Controllability And Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells For Scan Design. Board Level And System Level DFT Approaches.

UNIT- V

BOUNDARY SCANS STANDARDS AND BIST: Compression Techniques – DifferentTechniques, Syndrome Test And Signature Analysis, BIST Concepts And Test Pattern Generation. Specific BIST Architectures CSBL, BEST, RTS, LOCST, STUMPS,CBIST, CEBS, RTD, SST,CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts And Design for Self-Test at Board Level.

UNIT- VI

MEMORY BIST (MBIST): Memory Test Architectures And Techniques – Introduction toMemory Test, Types Of Memories And Integration, Embedded Memory Testing Model, Memory Test Requirements for MBIST, Brief Ideas on Embedded Core Testing, Introduction to Automatic In Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House,2001
2. Alfred Crouch, Design for Test for Digital ICs and Embedded core systems, Prentice Hall.

REFERENCES:

1. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing ,Prentice Hall,Englehood Cliffs,1998

Elective-IV

DSP PROCESSORS AND ARCHITECTURES

Credits: 3

Subject Code: MTVL – 2.4 **Max. Marks:** 70
II – Semester **Sessionals:** 30

UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES AND EXECUTION

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing, Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models

UNIT IV
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS AND FFT ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller,

Adaptive Filters, 2-D Signal Processing, An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum

UNIT VI
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications – B. VenkataRamani and M.Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

AUDIT COURSE

Credits: 0

Subject Code: MTVL – 2.5 **Exam Marks:** 70

Semester-II **Sessional:** 30

HDL PROGRAMMING LAB-II

Credits:2

Subject Code: MTVL – 2.6 **Exam Marks:10**0

Semester-II

MIXED SIGNAL SIMULATION LABORATORY

Credits : 2

Subject Code :MTVL –2.7 **Max. Marks :**100

II – Semester

Elective-IV

SYSTEM MODELLING & SIMULATION

Credits : 3

Subject Code :MTVL –3.1 **Max. Marks :**70
III – Semester **Sessionals :**30

UNIT I

Basic Simulation Modeling : Systems, Models and Simulation, Discrete Event Simulation,Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS AND MODELING TIME DRIVEN SYSTEMS:

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility. Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation

UNIT IV

EXOGENOUS SIGNALS AND EVENTS:

Disturbance signals, state machines, petri nets & analysis, System encapsulation, Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

UNIT V

EVEN DRIVEN MODELS:

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT VI

SYSTEM OPTIMIZATION:

System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

TEXT BOOKS:

1. System Modeling & Simulation, An introduction – Frank L.Severance, John Wiley&Sons, 2001.
2. Simulation Modeling and Analysis – Averill M.Law, W.David Kelton, TMH, 3rd Edition, 2003

REFERENCES:

1. Systems Simulation – Geoffery Gordon, PHI, 1978

Elective-IV

EMI / EMC

Credits : 3

Subject Code :MTVL –3.1 **Max. Marks :**70
III– Semester **Sessionals :**30

UNIT I

INTRODUCTION, NATURAL AND NUCLEAR SOURCES OF EMI / EMC:Electromagnetic Environment, History, Concepts, Practical Experiences and Concerns, Frequency Spectrum Conservations. An Overview of EMI / EMC, Natural and Nuclear Sources of EMI.

UNIT II

EMI FROM APPARATUS, CIRCUITS AND OPEN AREA TEST SITES:Electromagnetic Emissions, Noise from Relays and Switches, Nonlinearities in Circuits, Passive Intermodulation , Cross Talk in Transmission Lines, Transients in Power Supply Lines, Electromagnetic Interference (EMI). Open -Area Test Sites and Measurements.

UNIT III

RADIATED AND CONDUCTED INTERFERENCE MEASUREMENTS AND ESD:Anechoic Chamber, TEM Cell, Giga-Hertz TEM Cell, Characterization of Conduction Currents / Voltages, Conducted EM Noise on Power Lines, Conducted EMI from Equipment, Immunity to Conducted EMI Detectors and Measurements. ESD, Electrical Fast Transients / Bursts, Electrical Surges.

UNIT IV

GROUNDING, SHIELDING, BONDING AND EMI FILTERS: Principles and Types ofGrounding, Shielding and Bonding, Characterization of Filters, Power Line Filter Design.

UNIT V

CABLES, CONNECTORS, COMPONENTS AND EMC STANDARDS: EMISuppression Cables, EMC Connectors, EMC Gaskets, Isolation Transformers, Opto-Isolators, National/ International EMC Standards.

TEXT BOOKS:

1. Engineering Electromagnetic Compatibility by Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT– Delhi, Modules1– 9.

REFERENCE :

1. Introduction to Electromagnetic Compatibility, Ny, John Wiley, 1992, by C.R. Pal.

Elective-IV
HARDWARE SOFTWARE CO DESIGN

Subject Code :MTVL –3.1 **Max. Marks :**70
III– Semester **Sessionals :**30

Open Elective

CELLULAR AND MOBILE COMMUNICATIONS

Credits: 3

Subject Code :MTVL – 3.2 **Max. Marks :**70
II – Semester **Sessionals :**30

UNIT- I

Introduction to Wireless communications, examples of wireless communication system, the Cellular concept and system design fundamentals, Frequency reuse, channel assignment strategies, handoff strategies, Interference and system capacity, Trunk and grade services, Methods for improving coverage and capacity in cellular system

UNIT- II

Multiple access techniques for wireless communications FDMA, TDMA, Spread spectrum techniques, SDMA, Packet Radio, CSMA , Capacity of cellular CDMA with multiple cells and capacity of SDMA.

UNIT-III

Wireless systems and standards, AMPS, IS – 94, GSM traffic, Examples of GSM cell, Frame structure of GSM cell, Details of forward and reverse CDMA channels.

UNIT-IV

Personal access communication systems, personal Mobile satellite communications, Integrating Geo, LEO MEO satellite and terrestrial mobile systems, Rake receiver and Advanced Rake receiver,

UNIT-V

Mobile Radio Propagation, Large scale path loss, Reflection, Diffraction, Scattering, Outdoor and Indoor Propagation models, small signal fading and multi path, measurement of small scale path loss, parameters and multi path channels, fading due to multi path, fading effect due to Doppler spread, small scale fading models, equalization, Diversity.

Text Book:

1. Mobile cellular communication by GottapuSasibhushan Rao, PERSON International, 2012.
2. Wireless communications Principles and Practice, Second Editions, THEODORE S.REPPAPORT.

REFERENCES:

1. Wireless Digital Communications, DR. KAMILO FEHER.
2. Electronic Communication system, WAYNE ToMASI.
3. Wireless Communications, SANJY SHARMS