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(57) Abstract :
Exemplary aspects of the present disclosure are directed toward AN FPGA-BASED SYSTEM FOR THE REALIZATION OF CDMA TECHNIQUE, a kind of electronic device capable of effective analysis of one or more parameters including collecting data for noise analysis. Further, the device incorporates Network on Chip (NoC) CDMA architecture for the realization of different CDMA techniques, wherein P2S (Parallel to Serial) and S2P (Serial to Parallel) converters are used in transmitting and receiving blocks. Eight nodes, the SBCDMA method and WBCDMA were implemented on the device to lead to the understanding that SBCDMA has reduced power dissipation by 64.87%, LUT count by 49.8% and latency by 45% over WBCDMA.

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